Appl. No. 10/694,155
Examiner: CHEN, JACK S J, Art Unit 2813
In response to the Office Action dated December 6, 2004

Date: March 5, 2005
Attorney Docket No. 10110752

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method for fabricating a vertical nitride read-only memory (NROM) cell, comprising the steps of:

providing a substrate having at least one trench;

forming doping areas as bit lines in the substrate near its surface and the bottom of the trench;

forming bit line oxides over each of the doping areas;

forming a conformable insulating layer as gate dielectric on and in direct contact with the substrate surface that constitutes sidewalls of the trench and the surface of the bit line oxide; and

forming a conductive layer as a word line over the insulating layer and filling in the trench.

Claim 2 (original): The method as claimed in claim 1, wherein the trench has a depth of about 1400~1600 Å.

Claim 3 (original): The method as claimed in claim 1, wherein formation of the doping areas further comprises:

forming a spacer over the sidewall of the trench; and

performing ion implantation in the substrate using the spacer as a mask.

Claim 4 (original): The method as claimed in claim 3, wherein the spacer is silicon nitride.

Claim 5 (original): The method as claimed in claim 3, wherein the ion implantation is performed by phosphorus.

Claim 6 (original): The method as claimed in claim 3, further removing the spacer before formation of the conformable insulating layer.

Claim 7 (original): The method as claimed in claim 1, wherein the bit line oxides are formed by thermal oxidation.

Claim 8 (original): The method as claimed in claim 1, wherein the bit line oxides have a thickness of about 500~700 Å.

Claim 9 (original): The method as claimed in claim 1, wherein the insulating layer is an oxide-nitride-oxide layer.

Claim 10 (original): The method as claimed in claim 1, wherein the conductive layer is polysilicon.